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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,590	07/30/2003	Shin Fujita	116725	6224

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EXAMINER	
BODDIE, WILLIAM	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/629,590	FUJITA, SHIN	
	Examiner	Art Unit	
	William L. Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☒ Claim(s) 12 and 13 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 December 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____. 10/20/03, 6/15/06, 9/22/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: _____. Fujita translation

DETAILED ACTION

Claim Objections

1. Claims 12-13 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

2. Specifically, claims 12-13 contradict limitations from claim 1 which they are dependent from, as such they fail to further limit claim 1.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-16 recite the limitation "the first correction circuit and the second correction circuit" in line 13 of claim 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yukinori (JP 08-065113) in view of Murade (JP 11-282397).

With respect to claim 1, Yukinori discloses, a timing adjustment circuit (fig. 2) that receives an input positive-logic signal (AI in fig. 4) that is asserted at its high level (clear from fig. 4), and an input positive-logic signal (BI in fig. 4) that is asserted at its high level (clear from fig. 4), and that generates an output positive-logic signal and an output negative-logic signal that have their phase difference decreased (para. 2), comprising:

a signal generation portion that generates a reference signal (AI in fig. 4) on the basis of either of the input positive-logic signal and the input negative-logic signal, and that generates a signal to-be-corrected on the basis of the other signal (col. 5, lines 41-44); and

a correction portion (22 and 24 in fig. 2) that corrects the signal to-be-corrected on the basis of the reference signal;

said reference signal being delivered as one of the output positive-logic signal 7and the output negative-logic signal (AO in fig. 4), while a signal obtained by correcting said signal to-be-corrected by the first correction circuit and the second correction circuit is delivered as the other of said output positive-logic signal and said output negative-logic signal (BO in fig. 4).

Yukinori does not expressly disclose, that the input and output signals are differing logic types, or a signal generation portion.

Murade discloses, a timing adjustment circuit (fig. 3) that receives an input positive-logic signal (CL in fig. 3) and an input negative logic signal (CLinv in fig. 3; note figs. 2b), wherein the signals are generated by a signal generation portion (501 in fig. 3)

that generates a reference signal (d1 in fig. 3) on the basis of either of the input positive-logic signal, and that generates a signal to-be-corrected (d6 in fig. 3) on the basis of the other signal (clear from fig. 3).

Murade and Yukinori are analogous art because they are both from the same field of endeavor namely timing adjustment devices.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the input signals of Yukinori with those of Murade and generate the reference signal and signal to be corrected as taught by Murade.

The motivation for doing so would have been to abolish phase contrast and apply positive feedback to the correction portion (Murade; para. 43).

With respect to claim 11, Yukinori and Murade disclose, the timing adjustment circuit as defined in claim 1 (see above).

Murade further discloses, wherein said signal generation portion includes a first inversion circuit (501a in fig. 2,3) which inverts either of said input positive-logic signal and said input negative-logic signal, thereby to generate said reference signal, and a second inversion circuit (501b in fig. 2,3) which inverts the other signal, thereby to generate said signal to-be-corrected (generation should be clear to fig. 3 and 2b).

With respect to claims 14-16, Yukinori and Murade disclose the timing adjustment circuit as defined in claim 1 (see above), wherein the timing of a predetermined signal (signal to be corrected) is adjusted using the timing adjustment circuit.

Murade further discloses, a drive circuit (500, 101 etc. in fig. 1) which drives an electro-optic device (para. 1) having a plurality of scanning lines (y1-ym in fig. 1), a plurality of data lines (s1-sn in fig. 1), and pixel electrodes (11 in fig. 1) and switching elements (30 in fig. 1) that are arranged in the shape of a matrix in correspondence with intersections between the scanning lines and the data lines (clear from fig. 1).

At the time of the invention it would have been obvious to one of ordinary skill in the art to use the combined timing adjustment device of Yukinori and Murade in an electro-optic device as taught by Murade.

The motivation for doing so would have been the dependence of electro-optic devices on exact timing signals (Murade; paras. 6-7).

7. Claims 2-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yukinori (JP 08-065113) in view of Murade (JP 11-282397) and further in view of Fujita (JP 2001-166744).

With respect to claim 2, Yukinori and Murade disclose, the timing adjustment circuit according to claim 1 (see above).

Yukinori further discloses, correcting the timing of said signal-to-be-corrected on the basis of the timing of said reference signal (clear from fig. 4 and 13b).

Neither Yukinori nor Murade expressly disclose, correcting the falling and leading edges of said signal-to-be-corrected on the basis of the leading and falling edges of the reference signal, respectively.

Fujita discloses, a correction portion (1464, 1474 in fig. 2) including:

a first correction portion (1464) that corrects a timing of a trailing edge of a signal to-be-corrected (P1) on the basis of a leading edge of a reference signal (P2); and

a second correction portion (1474) that corrects a timing of a leading edge of said signal to-be-corrected on the basis of a trailing edge of said reference signal (note the correction of the signals, in fig. 6, as they work through the circuitry of fig. 2).

Yukinori, Murade and Fujita are analogous art because they are from the same field of endeavor namely, timing adjustment circuits.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the logic circuits of Yukinori and Murade with those of Fujita.

The motivation for doing so would have been to correct timing signals so as to ensure that the outputs do not overlap, thereby increasing the quality of the displayed image (Fujita; para. 16-18).

With respect to claim 3, Yukinori, Murade and Fujita disclose, the timing adjustment circuit as defined in claim 2 (see above).

Fujita further discloses, wherein either of said correction portion and said second correction portion being a NAND circuit (1464 in fig. 2), while the other is a NOR circuit (inverting both inputs of an AND gate is equivalent logically to a NOR circuit).

With respect to claim 4, Yukinori, Murade and Fujita disclose, the timing adjustment circuit as defined in claim 3 (see above).

Fujita further discloses, a first wiring line that is fed with said reference signal (P2 in fig. 2); and

a second wiring line that is fed with said signal to-be-corrected (Q1, S1 and P1 in fig. 2);

one input terminal of said NAND circuit begin coupled to said first wiring line, while the other input terminal thereof is coupled to said second wiring line (clear from fig. 2), and an output terminal of said NAND circuit is coupled to said second wiring line (Q1 in fig. 2); and

one input terminal of said NOR circuit being coupled to said first wiring line (right input of 1474 in fig .2), while the other input terminal thereof being coupled to said second wiring line (Q1 in fig. 2), and an output terminal of said NOR circuit being coupled to said second wiring line (S1 in fig. 2).

With respect to claims 5 and 8, Yukinori, Murade and Fujita disclose, the timing adjustment circuit as defined in claim 2 (see above).

Yukinori further discloses, the reference signal (AI in figs. 4,5) both advancing (fig. 4) and retarding (fig. 5) in phase relative to said signal-to-be-corrected.

With respect to claims 6-7 and 9-10, Yukinori, Murade and Fujita disclose, the timing adjustment circuits as defined in claims 5 and 8 (see above).

As to limitations asserting the reference signal at a high or low level and vice versa for the signal-to-be-corrected, Yokoyama discloses it is obvious to those of ordinary skill in the art to reverse the logic states of each of the signals as needed by future circuits (col. 5, lines 35-54). In doing so Yokoyama also discloses instituting equivalent circuitry (col. 5, lines 49-54).

Yukinori, Murade and Yokoyama are analogous art because they are from the same field of endeavor namely, timing adjustment circuits.

At the time of the invention it would have been obvious to one of ordinary skill in the art to adjust the phases of the timing signals of Yukinori and Murade as taught by Yokoyama.

The motivation for doing so would have been simpler circuit design and to generate output signals as appropriate for constitute equivalent circuits (Yokoyama; col. 5, lines 48-49).

8. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yukinori (JP 08-065113) in view of Murade (JP 11-282397) and further in view of Houston (US 5,396,110).

With respect to claim 12, Yukinori and Murade disclose, the timing adjustment circuit as defined in claim 1 (see above).

Neither Yukinori nor Murade expressly disclose,

a single input being fed to said signal generation portion instead of said input positive-logic signal and said negative logic signal;

said signal generation portion generating said reference signal and said signal to-be-corrected on the basis of the input signal.

Houston discloses, a single input (IN in fig. 14) being fed to said signal generation portion (fig. 14) instead of said input positive-logic signal and said negative logic signal;

said signal generation portion generating a reference signal (output of 52 in fig. 14) and said signal to-be-corrected (output of 2nd 54 in fig. 14) on the basis of the input signal (clear from fig. 14).

Yukinori, Murade and Houston are analogous art because they are from the same field of endeavor namely, timing adjustment circuits.

At the time of the invention it would have been obvious to one of ordinary skill in the art to generate the input signals of Yukinori and Murade as taught by Houston.

The motivation for doing so would have been simpler circuit design and to lessen manufacturing costs by removing an entirely separate signal generation portion.

With respect to claim 13, Yukinori, Houston and Murade disclose, the timing adjustment circuit as defined in claim 12 (see above).

Houston further discloses, said signal generation portion including:

a first inversion circuit (52 in fig. 14) that inverts said input signal at least once, thereby to generate said reference signal; and

a second inversion circuit (54 in fig. 14) that inverts said input signal more than the number of times of inversion of said first inversion circuit, thereby to generate said signal to-be-corrected (clear from fig. 14).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William L. Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Wlb
3/30/07

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